JTO 深圳市晶腾光电有限公司

SHENZHEN JINGTENG OPTOELECTRONICS Co., LTD.

Product Specification For LCD Module

Model NO.：JTOTFT35312001A

REVISION：1

☐APPROVAL FOR SPECIFICATIONS ONLY

■APPROVAL FOR SPECIFICTAIONS AND SAMPLE

CUSTOMER：	APPROVED BY：

HUARI LCM R&D CENTER			
APPROVED BY	CHECKED BY	PREPARED BY	
ZHANG	MARKE		MARKE
DIRECTOR	MANAGER	Mechanism Engineer	Electronic Engineer

深圳市晶腾光电有限公司
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RECORD OF REVISION

REV	COMMENT	PAGE	DATE
1	Initial Release	1-20	2014/01/06

MODEL LABEL NUMBERING SYSTEM

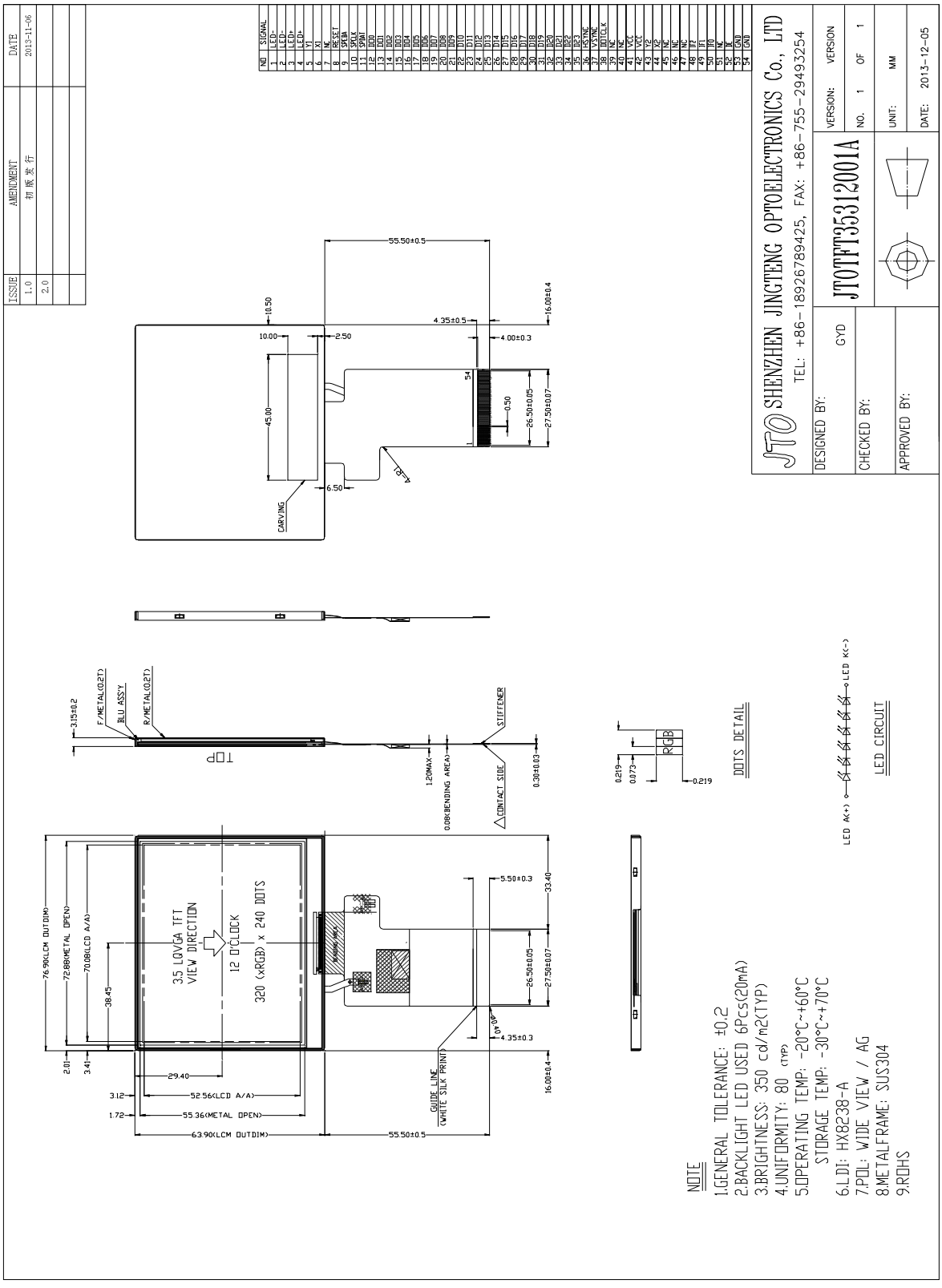
JTO FSTN 19296 3 10 001 A

- Edition: A~Z
- sequence: 001~999
- Month: 1~12
- particular year: 0~TBD
- SID DOT.
- Display Type: FSTN;HTN; TN; STN； TFT
- JTO： **SHENZHEN JINGTENG OPTOELECTRONICS Co., LTD.**

GENERAL SPECIFICATION

ITEM	CONTENTS
Module Size	76.9(W) × 63.9(H) × 3.15(T) mm
Display Format	320× 240 DOTS
View Area	72.88 (W) × 55.36(H) mm
Dot Size	-
Dot Pitch	0.108mm * 0.108mm
LCD Type	TFT
View Angle	12 O'clock
Controller IC	HX8238-D
Duty Ratio	-
Bias	-
Backlight Driver type	External Power
DC to DC circuit	Build-In
Weight	--

LCM DRAWING


JTO SHENZHEN JINGTENG OPTOELECTRONICS Co., LTD
TEL: +86-18926789425, FAX: +86-755-29493254
JTOTFT35312001A
3.5 LQVGA TFT
VIEW DIRECTION
12 O'CLOCK
320 (xRGB) x 240 DOTS
TOP
DOTS DETAIL
LED CIRCUIT
NOTE
1.GENERAL TOLERANCE: ±0.2
2.BACKLIGHT LED USED 6Pcs(20mA)
3.BRIGHTNESS: 350 cd/m2(TYP)
4.UNIFORMITY: 80 (TYP)
5.OPERATING TEMP: -20°C~+60°C
STORAGE TEMP: -30°C~+70°C
6.LDI: HX8238-A
7.POL: WIDE VIEW / AG
8.METALFRAME: SUS304
9.ROHS

ELECTRO-OPTICAL CHARACTERISTICS (Ta＝25℃)

ELECTRICAL SPECIFICATION

Item	Symbol	Specification			Unit
		Min.	Typ	Max.	
TFT gate on voltage	V_{GH}	-	+15	-	V
TFT gate off voltage	V_{GL}	-	-10	-	V
TFT common electrode voltage	V_{comH}	2.5	(3.6)	4.5	V
	V_{comL}	-3	(-2.4)	0	

Note: (1) Vcom must be adjusted to optimize display quality: cross talk, contrast ratio and etc.

(2) VGH is TFT gate operating voltage

(3) VGL is TFT gate operating voltage

(4) Environmental condition: 25±5℃

BACKLIGHT

PARAMETER	Sym.	Min.	Typ.	Max.	Unit	Test Condition	Note
Supply Current	I	-	20	-	mA		
Supply Voltage	V	18	-	-	V	-	
Luminous Intensity IV	-			350	Cd/m^2		
Uniformity	-	80	--	-	%		
Chromaticty Coordinate	X	0.28		0.31	nm		
	Y	0.29	--	0.32	nm		
Color	White						

LCD OPTICALCHARACTERISTICS/COLOROFCIECOORDINATE

Item		Symbol	Conditions	Specifications Min.	Typ.	Max.	Unit	Note
Transmittance		T%	Viewing normal angle $\theta_X = \theta_Y = 0°$		7.4		%	All left side data are based on CMO's following condition –T6 NTSC: 60% LC:5091 Light : C light (Machine:BM5A) Normal Polarizer Without DBEF "Simulation Data Reference Only"
Contrast Ratio		CR		200	300		--	
Response Time		T_R			15	30	ms	
		T_F			35	50	ms	
Chromaticity	Red	X_R		0.609	0.639	0.669		
		Y_R		0.314	0.344	0.374		
	Green	X_G		0.264	0.294	0.324		
		Y_G		0.557	0.587	0.617		
	Blue	X_B		0.102	0.132	0.162		
		Y_B		0.106	0.136	0.166		
	White	X_W		0.282	0.312	0.342		
		Y_W		0.319	0.349	0.379		
Viewing Angle	Hor.	θ_{X+}	Center CR≥10		45		deg.	
		θ_{X-}			45			
	Ver.	θ_{Y+}			15			
		θ_{Y-}			35			

*Note (1) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L63 / L0

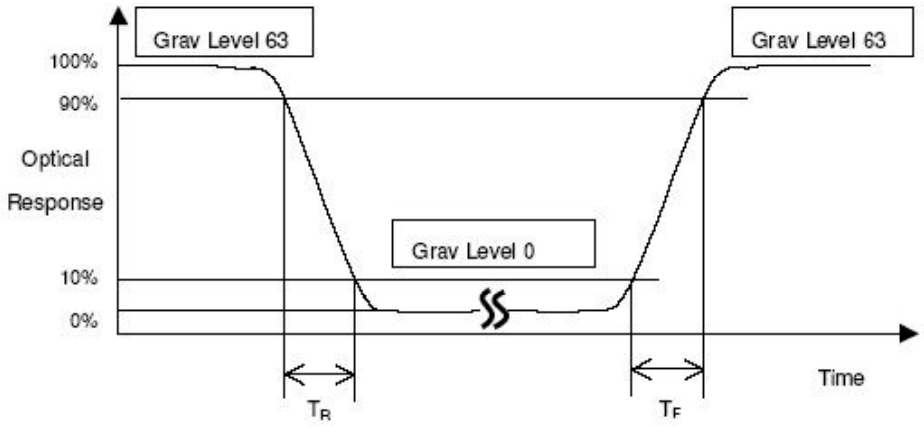
L63: Luminance of gray level 63

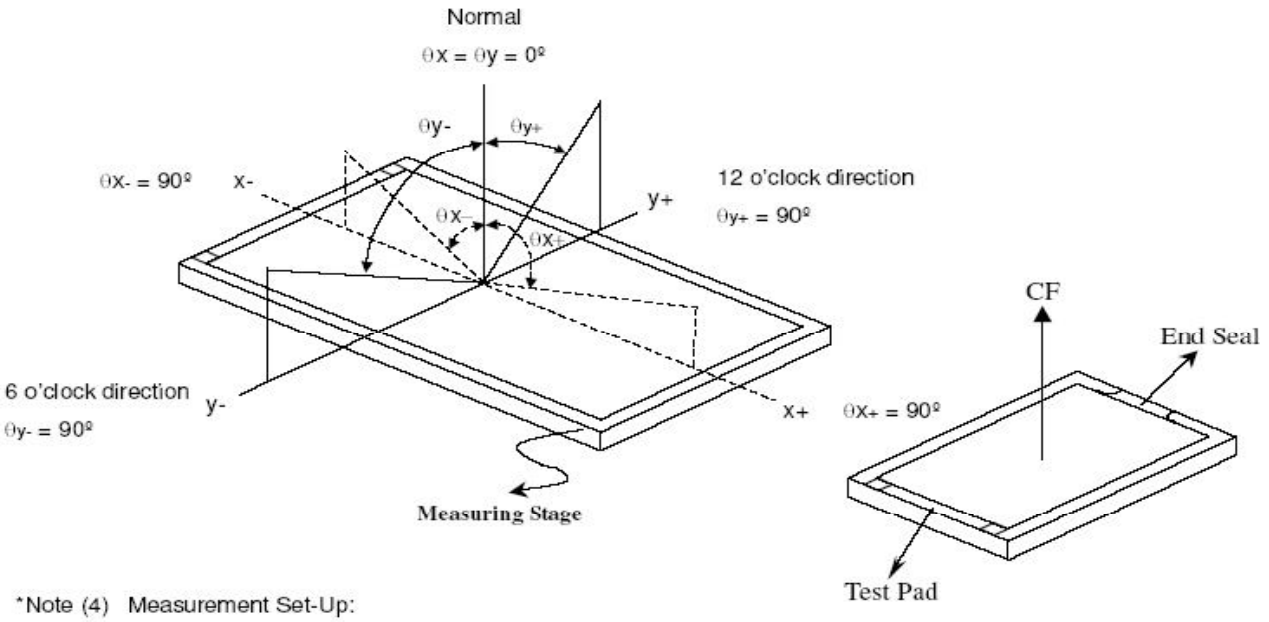
L 0: Luminance of gray level 0

CR = CR (10)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

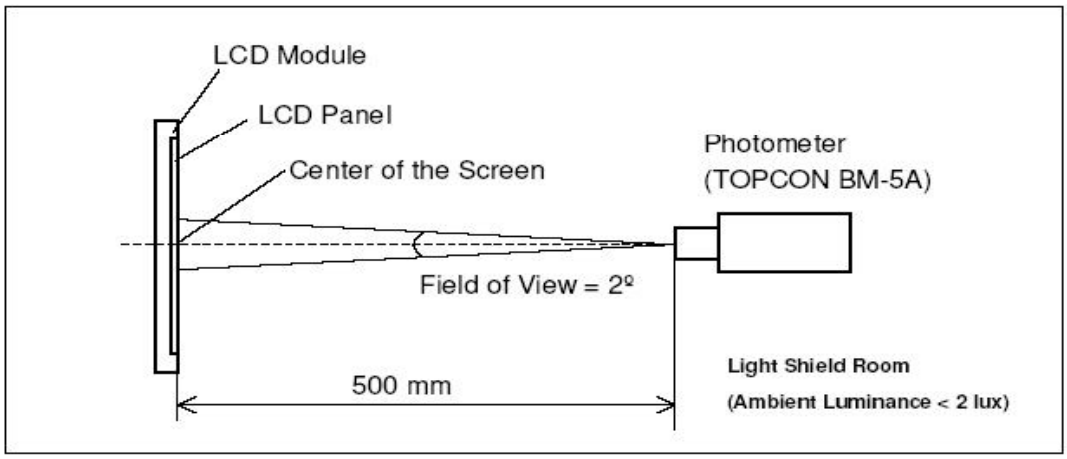
*Note (2) Definition of Response Time (T_R, T_F):

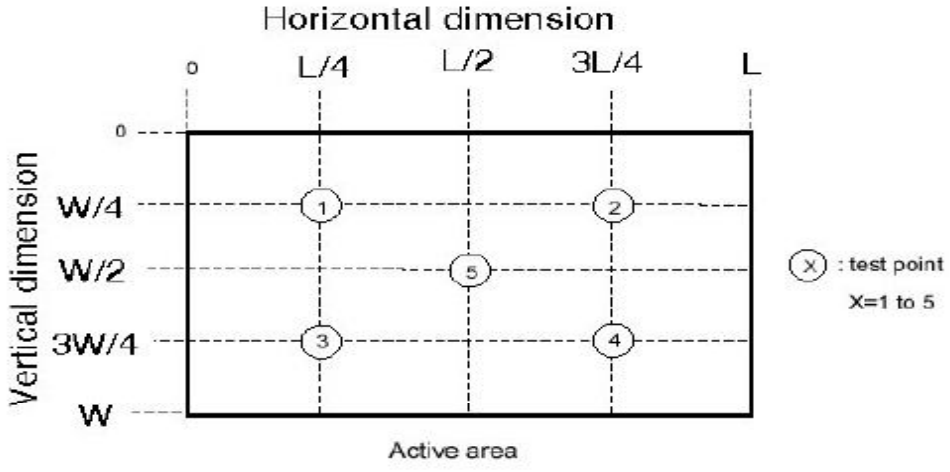




*Note (4) Measurement Set-Up:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.





INTERFACE PIN ASSIGNMENT

PIN	SYMBOL	FUNCTIONS
1	LED_CATHOD	LED Light Power Supply .0V
2	LED_CATHOD	LED Light Power Supply .0V
3	LED_ANODE	LED Light Power Supply .19.2V
4	LED_ANODE	LED Light Power Supply .19.2V
5	Y1	Top electrode
6	X1	Right electrode
7	NC	Not use
8	REST	This signal will reset the device and must be applied to properly initialize the chip
9	SPENA	Chip select input PIN of serial interface
10	SPCLK	Clock PIN of serial interface
11	SPAD	Data input pin in serial interface
12~35	D0~D23	Data Bit0 ~Data Bit23
36	HSYNC	Horizontal sync signal in RGB I/F
37	VSYNC	Vertical sync signal in RGB I/F
38	DOTCLK	Pixel clock signal in RGB I/F
39	NC	Not use
40	NC	Not use
41	VDD	Power Supply For Logic
42	VDD	Power Supply For Logic
43	Y2	Bottom electrode
44	X2	Left electrode
45	NC	Not use
46	NC	Not use
47	NC	Not use
48	IF2	Control the input data format
49	IF1	Control the input data format
50	IF0	Control the input data format
51	NC	Not use
52	DEN	Data enable signal in RGB I/F
53	GND	This is a 0V terminal connected to the system GND.
54	GND	This is a 0V terminal connected to the system GND.

AC TIMING CHARACTERISTICS

AC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 2.2V, T_A = 25℃)

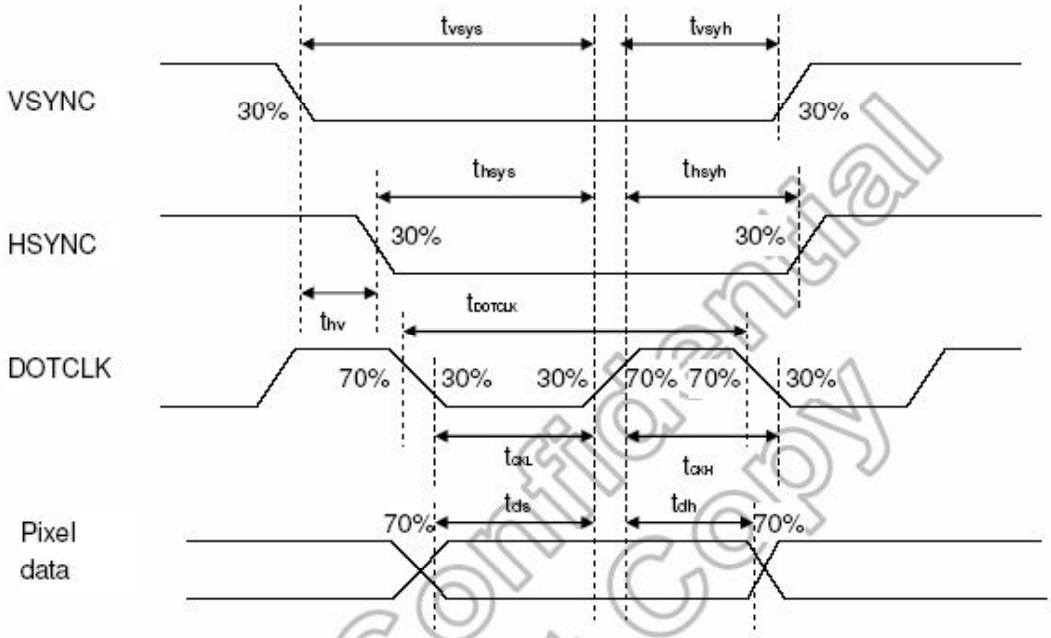


Figure13. 1 Pixel Timing

Characteristics	Symbol	Min.		Typ.		Max.		Unit
		24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency	fDOTCLK	-		6.5	19.5	10	30	MHz
DOTCLK Period	tDOTCLK	100	33.3	154	51.3	-	-	ns
Vertical Sync Setup Time	tvsys	20	10	-	-	-	-	ns
Vertical Sync Hold Time	tvsyh	20	10	-	-	-	-	ns
Horizontal Sync Setup Time	thsys	20	10	-	-	-	-	ns
Horizontal Sync Hold Time	thsyh	20	10	-	-	-	-	ns
Phase difference of Sync Signal Falling Edge	thv	1		-		240		tDOTCLK
DOTCLK Low Period	tCKL	50	15	-	-	-	-	ns
DOTCLK High Period	tCKH	50	15	-	-	-	-	ns
Data Setup Time	tds	12	10	-	-	-	-	ns
Data hold Time	tdh	12	10	-	-	-	-	ns
Reset pulse width	tRES	10		-		-		us

Note: External clock source must be provided to DOTCLK pin of HX8238-A. The driver will not operate if absent of the clocking signal.

Table 13. 1 Pixel Timing

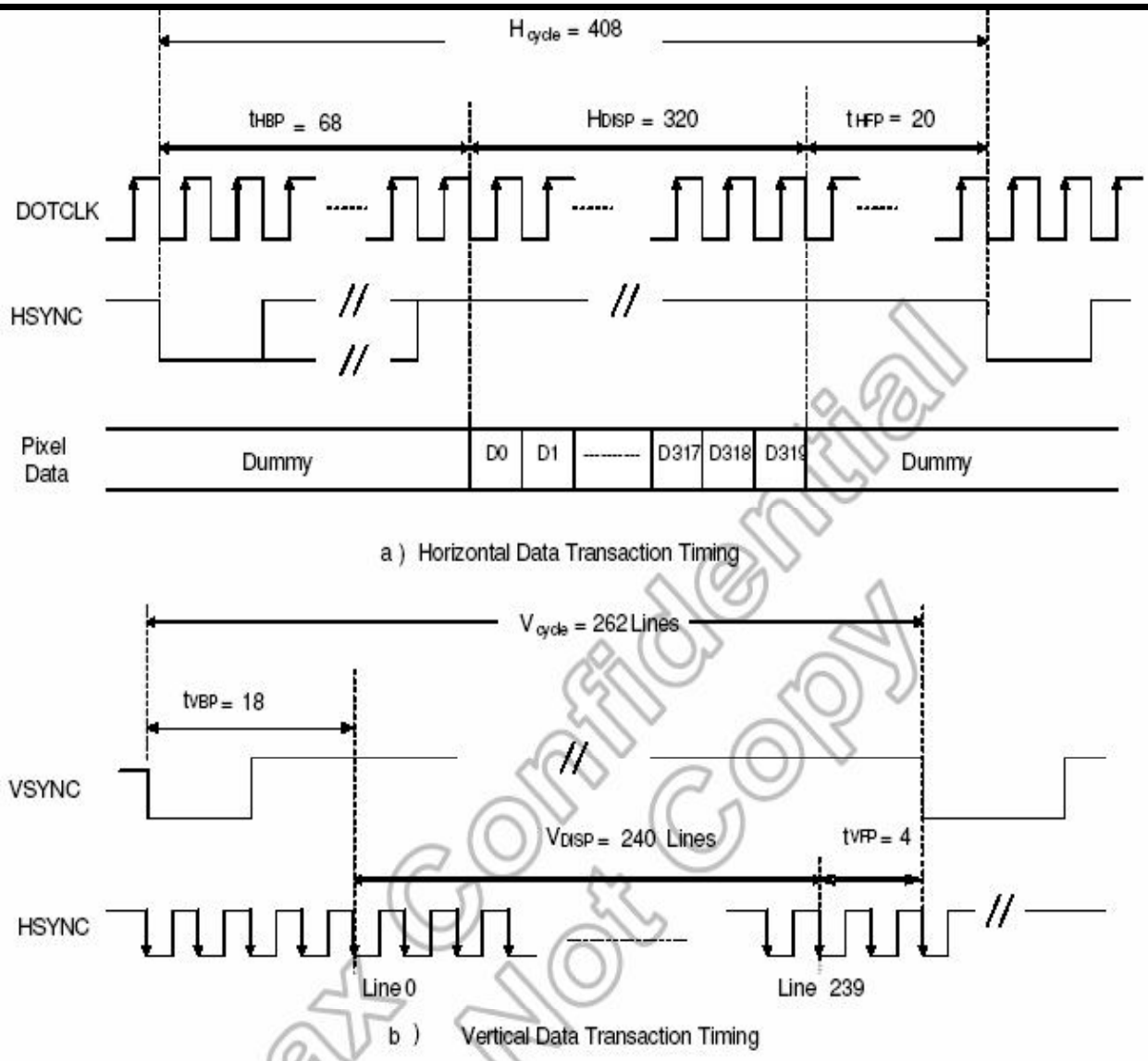


Figure13. 2 Data Transaction Timing in Parallel RGB (24 bit) Interface (SYNC Mode)

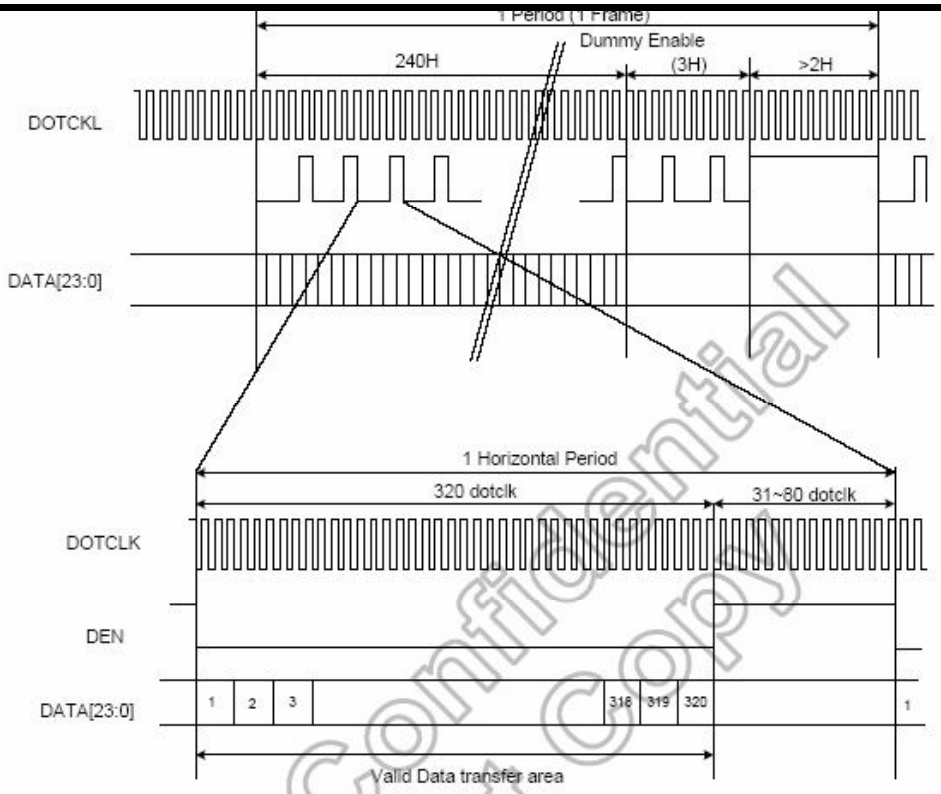


Figure13. 3 Data Transaction Timing in Parallel RGB (24 bit) Interface (DE Mode)

Characteristics		Symbol	Min.		Typ.		Max.		Unit
			24 bit	8 bit	24 bit	8 bit	24 bit	8 bit	
DOTCLK Frequency		fDOTCLK	-	-	6.5	19.5	10	30	MHz
DOTCLK Period		tDOTCLK	100	33.3	154	51.3	-	-	ns
Horizontal Frequency (Line)		fH	-		14.9		22.35		KHz
Vertical Frequency (Refresh)		fV	-		60		90		Hz
Horizontal Back Porch		tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Front Porch		tHFP	-	-	20	60	-	-	tDOTCLK
Horizontal Data Start Point		tHBP	-	-	68	204	-	-	tDOTCLK
Horizontal Blanking Period		tHBP + tHFP	-	-	88	264	-	-	tDOTCLK
Horizontal Display Area		HDISP	-	-	320	960	-	-	tDOTCLK
Horizontal Cycle		Hcycle	-	-	408	1224	450	1350	tDOTCLK
Vertical Back Porch		tVBP	-		18		-		Lines
Vertical Front Porch		tVFP	-		4		-		Lines
Vertical Data Start Point		tVBP	-		18		-		Lines
Vertical Blanking Period		tVBP + tVFP	-		22		-		Lines
Vertical Display Area	NTSC	VDISP	-		240		-		Lines
	PAL				280(PALM=0)				
					288(PALM=1)				
Vertical Cycle	NTSC	Vcycle	-		262		350		Lines
	PAL				313				

Table 13. 2 Data Transaction Timing in Normal Operating Mode

DC CHARACTERISTICS

DC Characteristics

(Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DDIO} = 2.2V, T_A = 25℃)

Symbol	Parameter	Test condition	Spec.			Unit
			Min	Typ	Max	
V_{DD}	System power supply pins of the logic block	Recommend Operating Voltage Possible Operating Voltage	1.8	-	2.50	V
V_{DDIO}	Power supply pin of IO pins	Recommend Operating Voltage Possible Operating Voltage	1.8	-	3.6	V
V_{CI}	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	2.5 or VDDIO	-	3.6	V
I_{sleep}	Sleep mode current	-	-	50		μA
I_{dp}	Operating mode current	VCI=3.3V	-	10	12	mA
V_{CIM}	Negative V_{CI} Output Voltage	No panel loading	- VCI	-	- VCI+0.7	V
V_{CIX2}	V_{CIX2} primary booster efficiency(1)	No panel loading, ITO for V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	83	90	-	%
V_{GH}	Gate driver High Output Voltage Booster efficiency(2)	No panel loading; 4x booster; ITO for C_{YP}, C_{YN}, V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	84	89.5	-	%
		No panel loading; 5x booster; ITO for C_{YP}, C_{YN}, V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	80	88.5	-	%
		No panel loading; 6x booster; ITO for C_{YP}, C_{YN}, V_{CIX2}, V_{CI} and V_{CHS} = 10 Ohm	72	80	-	%
V_{GL}	Gate driver Low Output Voltage	-	- V_{GH}	-	-5.1	V
V_{COMH}	VCOM High Output Voltage	-	-	-	5.56	V
V_{COML}	VCOM Low Output Voltage	-	V_{CIM}+0.2	-	-	V
V_{COMA}	VCOM Amplitude	-	-	-	6	V
V_{LCD63}	V_{LCD63} Output Voltage	-	-	-	5.59	V
$\triangle V_{LCD63}$	Max. Source Voltage Variation	-	-2	-	2	%
V_{OH1}	Logic High Output Voltage	I out = -100μA	0.9*V_{DDIO}	-	V_{DD}	V
V_{VD}	Source Output Voltage Deviation	-	-	±20	-	mV
V_{OS}	Source Output Voltage Offset	-	-	-	±30	mV
V_{OL1}	Logic Low Output Voltage	I out = 100μA	0	-	0.1*V_{DDIO}	V
V_{IH1}	Logic High Input voltage	-	0.8*V_{DDIO}	-	V_{DDIO}	V
V_{IL1}	Logic Low Input voltage	-	0	-	0.2*V_{DDIO}	V
I_{OH}	Logic High Output Current Source	V out = VDD – 0.4V	50	-	-	μA
I_{OL}	Logic Low Output Current Drain	V out = 0.4V	-	-	-50	μA
I_{OZ}	Logic Output Tri-state Current Drain Source	-	-1	-	1	μA
$I_{IL/IH}$	Logic Input Current	-	-1	-	1	μA
C_{IN}	Logic Pins Input Capacitance	-	-	5	7.5	pF
R_{SON}	Source drivers output resistance	-	-	1	-	kΩ
R_{GON}	Gate drivers output resistance	-	-	500	-	Ω
R_{COM}	VCOM output resistance	-	-	200	-	Ω

Note : (1) VCIX2 efficiency = VCIX2 / (2 x VCI) x 100%
(2) VGH efficiency = VGH / (VCI x n) x 100% (where n = booster factor)

Table 12. 1 DC Characteristics

RELIABILITY

	No	Test Item	Content of Test	Test Condition
Environment Test	1	High Temperature Storage	Endurance test of high temperature for a long time.	60±2℃ 48H
	2	Low Temperature Storage	Endurance test of low temperature for a long time.	-20±2℃ 48H
	3	High Temperature Operation	Endurance test of electrical stress (Voltage & Current) and the thermal stress to the element.	60±2℃ 48H
	4	High Temperature /Humidity Storage	Endurance Test of high temperature and high humidity for a long time.	60±2℃ 60±2%RH 48H
	5	Thermal shock	Endurance test of low and high temperature cycles.(air to air) -20±2℃ ⟷ 60±2℃ (60min) ⟷ (60min) 1 cycle	-20±2℃/70±2℃ 10 cycle

Note: 1) When making the low temperature test, not to dewy.

2) Driving condition for operation test.

Power Supply Voltage for Logic System (VDD) =2.8V

Failure Judgment Criterion

After the above mentioned test.

(For Environmental Test, after 2 hours in room temperature.)

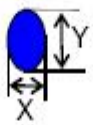
There should not be conspicuous failure of display quality and appearance.

2) Contrast ratio should be 50% of the initial contrast ratio.

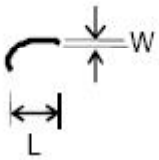
3) There should not have any abnormality of functions.

INSPECTION CRITERIA

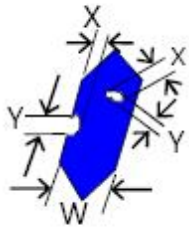
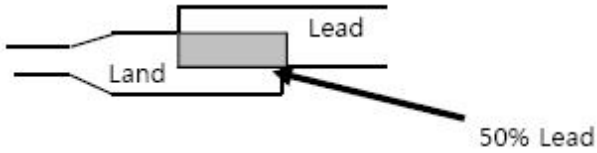
<table>
<tr><th>No.</th><th>Item</th><th>Criterion</th></tr>
<tr><td>1</td><td>Short or open circuit
LC leakage
Flickering
No display
Wrong viewing direction
Wrong Back-light</td><td>Not allow</td></tr>
<tr><td>2</td><td>Contrast defect
Background color deviation</td><td>Refer to approval sample</td></tr>
<tr><td>3</td><td>Point defect,
Black spot, dust
(including Polarizer)

$\phi = (X+Y)/2$</td><td> 

<table>
<tr><th>Point Size</th><th>Acceptable Qty.</th></tr>
<tr><td>$\phi \leq 0.10$</td><td>Disregard</td></tr>
<tr><td>$0.10 < \phi \leq 0.20$</td><td>3</td></tr>
<tr><td>$0.20 < \phi \leq 0.25$</td><td>2</td></tr>
<tr><td>$0.25 < \phi \leq 0.30$</td><td>1</td></tr>
<tr><td>$\phi > 0.30$</td><td>0</td></tr>
</table>
Unit：mm</td></tr>
<tr><td>4</td><td>Line defect,

Scratch</td><td> 

<table>
<tr><th colspan="2">Line</th><th>Acceptable Qty.</th></tr>
<tr><td>L</td><td>W</td><td></td></tr>
<tr><td>---</td><td>0.015≥W</td><td>Disregard</td></tr>
<tr><td>3.0≥L</td><td>0.03≥W</td><td rowspan="2">2</td></tr>
<tr><td>2.0≥L</td><td>0.05≥W</td></tr>
<tr><td>1.0≥L</td><td>0.1＞W</td><td>1</td></tr>
<tr><td>---</td><td>0.05<W</td><td>Applied as point defect</td></tr>
</table>
Unit：mm</td></tr>
<tr><td>5</td><td>Rainbow</td><td>Not more than two color changes across the viewing area.</td></tr>
</table>

No.	Item	Criterion
6	Segment pattern W = Segment width ϕ = (X+Y)/2	(1) Pin hole ϕ < is acceptable.  Point Size / Acceptable Qty ϕ≤1/4W / Disregard 1/4W< ϕ≤1/2W / 1 ϕ>1/2W / 0 Unit：mm
7	Back-light	(1) The color of backlight should correspond its specification. (2) Not allow flickering
8	Soldering	(1) Not allow heavy dirty and solder ball on PCB. (The size of dirty refer to point and dust defect) (2) Over 50% of lead should be soldered on Land. 
9	Wire	(1) Copper wire should not be rusted (2) Not allow crack on copper wire connection. (3) Not allow reversing the position of the flat cable. (4) Not allow exposed copper wire inside the flat cable
10	PCB	(1) Not allow screw rust or damage. (2) Not allow missing or wrong putting of component.
11	Total No. of Acceptable Defect	A Zone Maximum 2 minor non-conformities per one unit. Defect distance: each point to be separated over 10mm B. Zone It is acceptable when it is no trouble for quality and assembly in customer's end product.

Precaution for use of LCD module

11.1、Handling Precautions

1) The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

2) If the display panel is damaged and the liquid crystal substance inside it leaks out ,be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

3) Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

4) The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

5) If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

--Isopropyl alcohol

--Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer.

Especially, do not use the following:

--Water

--Ketone

--Aromatic solvents

6) Do not attempt to disassemble or process the LCD module.

11.2、Assembling Precautions

1) When mounting the LCD module make sure that it is free of twisting, warping, and distortion. Distortion has great influence upon display quality. Also keep the stiffness enough regarding the outer case.

2) Please handle the LCD module by its side.

3) NC terminal should be open. Do not connect anything.

4) If the logic circuit power is OFF, do not apply the input signals.

5) To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

·Be sure to ground the body when handling the LCD module.

·Tools required for assembly, such as soldering irons, must be properly grounded.

·To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

·The LCD module is coated with a film to protect the display surface. Exercise care when peeling off this protective film since static electricity may be generated.

6) Be careful when treating the glass panel because it has very sharpened edge.

11.3、Storage Precautions

1) When storing the LCD module, avoid exposure to direct sunlight of to the light of fluorescent lamps and high temperature/high humidity. Whenever possible, the LCD module should be stored in the same conditions in which they were shipped from our company.
2) Exercise care to minimize corrosion of the electrode. Corrosion of the electrodes is accelerated by water droplets or a current flow in a high-humidity environment.

4、Design Precautions

The absolute maximum ratings represent the rated value beyond which LCD module can not

1) exceed. When the LCD modules are used in excess of this rated value, their operation characteristics may be adversely affected.
2) To prevent the occurrence of erroneous operation caused by noise, attention must be paid to satisfy V_{IL}, V_{IH} specification values including taking the precaution of using signal cables that are short.
3) The LCD exhibits temperature dependency characteristics. Since recognition of the display becomes difficult when the LCD is used outside its designated operating temperature range, be sure to use the LCD within this range. Also keep in mind that the LCD driving voltage levels necessary for clear displays will vary according to temperature.
4) We recommended that power supply lines (VDD) have over-current protection line. (Fuse etc. Recommend Value:0.5A)
5) Sufficiently notice the mutual noise interference occurred by peripheral devices.
6) To cope with EMI, take measures basically on outputting side.
7) When installing an LCD module, fasten it at the LCD panel.
8) The display panel is made of general float glass which is not guaranteed for strength. So please consider about following.

Others

1) Liquid crystal solidifies under low temperature (below the storage temperature range) leading to defective orientation or the generation of air bubbles (black or white). Air bubbles may also be generated if the LCD module is subjected to a strong shock at a low temperature.
2) If the LCD modules have been operating for a long time showing the same display patterns, the display patterns may remain on the screen as ghost images and a slight contrast irregularity may also appear. A normal operating status can be regained by suspending use for some time. It should be noted that this phenomenon does not adversely affect performance reliability.
3) To minimize the performance degradation of the LCD module's resulting from destruction caused by static electricity, etc., exercise care to avoid touching the following section when handling this module: LCD's Terminal electrode sections.
4) Optimum voltage to obtain best contrast value depending on products. Therefore voltage adjustment with electric volume is required in each display.
5) Precaution for disposal of LCD module. When disposal of LCD module, ask specialization company of industrial waste which is permitted by the government. When burn up LCD module, obey the law of environmental hygienics. wash it off well with soap and water.